What is claimed is:

1. A circuit for use in a semiconductor memory, the device comprising:

a direct sense AMP circuit for transmitting read data loaded in a bit line pair including first and second bit lines to a data input/output line pair including first and second data input/output lines in response to a read command signal;

an input/output gate circuit for transmitting the read data loaded in the bit line pair to the data input/output line pair and for transmitting write data loaded in the data input/output line pair to the bit line pair, in response to a read/write signal.

2. The circuit of claim 1, further comprising:

an operation control unit for generating the read command signal and the read/write signal to turn ON both the direct sense AMP circuit and the input/output gate circuit in response to a column address signal and a write command in a data read operation, and for generating the read command signal and the read/write signal to turn ON the input/output gate circuit and to turn OFF the direct sense AMP circuit in a data write operation.

3. The circuit of claim 2, wherein the operation control unit generates the read command signal and the read/write signal at a first level in a data read operation and generates the read command signal at a second level and the read/write signal at the first level in a data write operation.

4. The circuit of claim 2, wherein the operation control unit generates both the read command signal and the read/write signal at the first level when the column address signal has the first level and the write command has the second level; and generates the read command signal at the second level and the read/write signal at the first level when both the column address signal and the write command have the first level.

5. The circuit of claim 1, wherein the input/output gate circuit comprises:

a first transistor having a first end connected to the first data input/output line, a second end connected to the first bit line, and a gate to which the read/write signal is applied; and

a second transistor having a first end connected to the second data input/output line, a second end connected to the second bit line and a gate to which the read/write signal is applied;

and wherein the direct sense AMP circuit comprises:

a first sense transistor having a first end connected to the first data input/output line and a gate connected to the second bit line;

a second sense transistor having a first end connected to the second data input/output line and a gate connected to the first bit line; and

a third sense transistor having a first end connected to second ends of the first sense transistor and the second sense transistor, a second end connected to a ground voltage, and a gate connected to the read command signal.

6. The memory circuit of claim 5, wherein at least one of the following is true: the first and second transistors are NMOS transistors; and the first through third sense transistors are NMOS transistors.

7. The memory circuit of claim 1, wherein the direct sense AMP circuit comprises:

a first sense transistor having a first end connected to a ground voltage and a gate connected to the second bit line;

a second sense transistor having a first end connected to the ground voltage and a gate connected to the first bit line;

a third sense transistor having a first end connected to a second end of the first sense transistor, a gate connected to the read command signal, and a second end connected to the first data input/output line; and

a fourth sense transistor which has a first end connected to a second end of the second sense transistor, a gate connected to the read command signal, and a second end connected to the second data input/output line.

8. The memory circuit of claim 7, wherein the memory is a Random Access Memory (RAM) or a Read Only Memory (ROM), and wherein the first through fourth sense transistors are NMOS semiconductor transistors.

9. A sense amplifying circuit for use in a semiconductor memory, the circuit comprising:

a direct sense AMP circuit adapted to transmit read data loaded in a bit line pair including first and second bit lines to a data input/output line pair including first and second data input/output lines when turned ON in response to a write block signal and a read/write signal in a data read operation, and which is turned OFF in response to the write block signal in a data write operation; and

an input/output gate circuit for transmitting the read data loaded in the bit line pair to the data input/output line pair in response to the read/write signal during the data read operation; and for transmitting write data loaded in the data input/output line pair to the bit line pair in response to the read/write signal during the data write operation.

10. The circuit of claim 9, wherein the direct sense AMP circuit comprises:

a first block transistor having a first end connected to the first data input/output line and a gate connected to the write block signal;

a second block transistor having a first end connected to the second data input/output line and a gate connected to the write block signal;

a first sense transistor having a first end connected to a second end of the first block transistor and a gate connected to the second bit line;

a second sense transistor having a first end connected to a second end of the second block transistor and a gate connected to the first bit line; and

a third sense transistor having a first end connected to second ends of the first sense transistor and the second sense transistor, a second end connected to a ground voltage, and a gate connected to the read/write signal.

11. The circuit of claim 10, wherein the first and second block transistors and the first through third sense transistors are NMOS semiconductor transistors.

12. The circuit of claim 9, wherein the direct sense AMP circuit comprises:

a first block transistor having a first end connected to the first data input/output line and a gate connected to the write block signal;

a second block transistor having a first end connected to the second data input/output line and a gate connected to the write block signal;

a first sense transistor having a first end connected to a second end of the first block transistor, and a gate connected to the second bit line;

a second sense transistor having a first end connected to a second end of the second block transistor, and a gate connected to the first bit line;

a third sense transistor having a first end connected to a second end of

the first sense transistor, and a gate connected to the read command signal;

a fourth sense transistor having a first end connected to a second end of the second sense transistor, and a gate connected to the read command signal.

13. The circuit of claim 9, wherein the input/output gate circuit comprises:

a first transistor having a first end connected to the first data input/output line, a second end connected to the first bit line, and a gate connected to the read/write signal; and

a second transistor having a first end connected to the second data input/output line, a second end connected to the second bit line, and a gate connected to the read/write signal.

14. The circuit of claim 13, wherein the first and second transistors are NMOS transistors.

15. The device of claim 10, wherein the read/write signal is a column address signal.

16. The circuit of claim 10, wherein the write block signal is generated at a first level in a data read operation and at a second level in a data write operation.

17. The circuit of claim 10, wherein the write block signal is generated by combining a write command with an address signal.

18. A sense amplifying circuit for use in a semiconductor memory, the circuit comprising:

a direct sense AMP circuit component adapted to transmit read data loaded in a bit line pair including first and second bit lines to a data input/output line pair including first and second data input/output lines, when turned ON in response to a read/write signal;

an input/output gate circuit adapted to pass the read data loaded in the bit line pair to the data input/output line pair in response to the read/write signal in the data read operation; and adapted to pass write data loaded in the data input/output line pair to the bit line pair in response to the read/write signal in the data write operation; and

a write/read control unit for passing the read data generated from the direct sense AMP circuit component to the data input/output line pair in response to a write block signal in the data read operation and for blocking connection between the direct sense AMP circuit component and the data input/output line pair in the data write operation.

19. The circuit of claim 18, wherein the write/read control unit comprises:

a first block transistor having a first end connected to the first data input/output line, a gate connected to the write block signal, and a second end connected to a first sense transistor in the direct sense AMP circuit component; and

a second block transistor having a first end connected to the second data input/output line, a gate connected to the write block signal, a second end connected to a second sense transistor in the direct sense AMP circuit component.

20. The circuit of claim 19, wherein the direct sense AMP circuit component comprises:

a first sense transistor having a first end connected to the second end of the first block transistor and a gate connected to the second bit line;

a second sense transistor having a first end connected to the second end of the second block transistor and a gate connected to the first bit line; and

a third sense transistor having a first end connected to second ends of the first sense transistor and the second sense transistor, a second end connected to a ground voltage, and a gate connected to the read/write signal.

21. The circuit of claim 20, wherein the first and second block transistors and the first through third sense transistors are NMOS transistors.

22. The circuit of claim 18, wherein the input/output gate circuit comprises:

a first transistor having a first end connected to the first data input/output line, a second end connected to the first bit line, and a gate connected to the read/write signal; and

a second transistor having a first end connected to the second data input/output line, a second end connected to the second bit line, and a gate connected to the read/write signal.

23. The circuit of claim 22, wherein the first and second transistors are NMOS transistors.

24. The circuit of claim 18, wherein the read/write signal is a column address signal, and the semiconductor memory is a Random Access Memory (RAM).

25. The circuit of claim 18, wherein the write block signal is generated at a first level in a data read operation and is generated at a second level in a data write operation.

26. The circuit of claim 18, wherein the write block signal is generated by combining a write command with an address signal.

27. The circuit of claim 18, wherein the semiconductor memory is a Read Only Memory (ROM).